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Conclusions on Code-Porting, Scaling and Optimization Workshops

Final

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Keywords:	PRACE, HPC, Research Infrastructure, Training, Education, Survey, Code-porting, Scaling, Optimization, Workshops
Abstract:	This deliverable reports on the four code-porting and scaling workshops held in Finland, Switzerland, Spain and Poland during 2009. The document outlines the workshop programmes and presents the outcomes and experiences from the hosting partners.

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References and Applicable Documents

[1] PRACE Deliverable D 3.3.1, *Survey of HPC Training and Education Needs* (June 2008)

List of Acronyms and Abbreviations

CUDA	Compute Unified Device Architecture
GPGPU	General-Purpose Graphic Processing Unit
GPU	Graphics Processing Unit
HPC	High Performance Computing; Computing at a high performance level at any given time; often used synonym with Supercomputing.
MPI	Message-Passing Interface; the standard specification for implementing message-passing in parallel systems.
OpenMP	OpenMP (Open Multi-Processing) is an application programming interface (API) that supports multi-platform shared memory multiprocessing programming in C/C++ and Fortran.
PRACE	Partnership for Advanced Computing in Europe; Project Acronym.
Tier-0	Denotes the apex of a conceptual pyramid of HPC systems. In this context the Supercomputing Research Infrastructure would host the tier-0 systems; national or topical HPC centres would constitute tier-1.
WP	Work Package
WP3	PRACE Work Package 3, *Training and Dissemination*
WP6	PRACE Work Package 6, *Software enabling for Petaflop/s systems*

Executive Summary

This report documents the organisation and outcomes of four PRACE code-porting and scaling workshops that were hosted during 2009. These workshops complete the PRACE HPC Training and Education programme, for the preparatory phase of the project, and significantly build upon the recommendations proposed within the PRACE HPC Training and Education survey [1].

The primary objective of these workshops was to provide participants with the necessary training, education and expertise to port and scale user applications to a broad spectrum of PRACE prototype petascale architectures, which may become resources within Europe's Tier-0 computing research infrastructure during the implementation phase of the PRACE project.

The workshops were hosted respectively by Finland, Switzerland, Spain and Poland and attracted more than 100 participants from across Europe, Asia and North America. The workshops provided students with access to four PRACE prototype systems (Cray XT5, NEC SX-9, BlueGene/P and IBM CELL) and the direct experience of 20 invited speakers who are renowned experts in porting and scaling applications to these architectures.

As well as the direct knowledge that was acquired during the workshop events, over 30 slide presentations were made available to the PRACE training portal, which captures the contents of the workshops for the entire HPC community. Furthermore, over 46 hours of edited, digital video recordings were obtained from the respective workshops which are also available, for on-demand online viewing, within the PRACE training portal, and provide the full workshop experience to the HPC community.

The overwhelming response from the participants of these workshops was positive and it is imperative that the PRACE Training and Education programme is further supported to provide similar events in the future. Without the transfer of knowledge from porting and scaling experts, users of forthcoming Tier-0 computing resources will be not be prepared adequately to exploit these valuable tools, in pushing the boundaries of European science and competing successfully within the global scientific community.

1 Introduction

The Partnership for Advanced Computing in Europe (PRACE) has the overall objective to prepare for the formation of a persistent pan-European HPC service. PRACE is a synergy of eight work packages spanning project management, legal formulation, training and dissemination, distributed computing and software and hardware for petascale computing.

Work package 3 (WP3) carries the responsibility for coordinating the dissemination of PRACE activities as well as steering and implementing the project's education and training programme for computational science aimed at scalable computing. As part of this training and education programme, WP3 was mandated to conduct four code-porting workshops across Europe with the specific aim of providing participants with the necessary skills to enable them to commence porting of their codes to the potential hardware architectures that are most likely to comprise the future PRACE Tier-0 computing infrastructure. With this valuable knowledge these European users will be in a better position to quickly accelerate their scientific output and therefore compete more readily within the global scientific community.

This document reports on the outcome of these workshops and provides some recommendations for future code-porting and scaling workshops that are envisaged as part of the continuing PRACE education and training programme.

The report is structured as follows:

- Chapter 2 describes the high-level organisation of the code-porting workshops and lists the PRACE partner sites who agreed to host a code-porting event;
- Chapter 3 details the individual workshop programmes;
- Chapter 4 presents conclusions on the code-porting workshop experiences and provides recommendations for similar events in future PRACE education and training programmes.

2 Organization and Promotion of Code-Porting Workshops

2.1 Hosting Sites

Four PRACE partners agreed to host a code-porting workshop during 2009. The partner affiliations, their hosting dates and locations are provided in Table 1.

Partner	Location	Date
CSC	Espoo, Finland	11th-12th June, 2009
CSCS	Manno, Switzerland	13th-15th July, 2009
ACC CYFRONET AGH	Cracow, Poland	14th-16th October, 2009
BSC	Barcelona, Spain	21st-23rd October, 2009

Table 1: PRACE Hosting Partners of Code-Porting Workshops

2.2 Workshop Programmes

Hosting partners were responsible for proposing their individual workshop programmes and inviting their nominated speakers within the context of the code-porting workshop requirements. To avoid unnecessary duplication of presentation material and target architectures at the individual workshops, a workshop organising committee was installed to oversee the event preparations. This committee was formed from the principal contacts at each hosting site under the chairmanship of Ari Turunen (WP3 Leader). The complete list of the committee members is presented in Table 2.

Hosting Site	Principal Contact
CSC, Finland	Ari Turunen (Chairman)
CSC, Finland	Sebastian von Alfthan
CSCS, Switzerland	Timothy Stitt
AGH, Poland	Lukasz Dutka
BSC, Spain	David Vicente

Table 2: Code-Porting Workshop Organising Committee

Meetings of the organising committee were more frequent at the beginning of 2009 as hosting sites worked diligently to design workshop programmes. As the workshop agendas neared completion, the necessity for meetings became less frequent. In addition to committee meetings, further discussions were held during periodic WP3 phone conferences and face-face meetings.

Due to the broad spectrum of participant nationalities expected at each code-porting event, it was agreed that the official language of each workshop was to be English.

2.3 Workshop Budgets

Each workshop site was allocated eight thousand (8000) Euro from within the WP3 budget to cover the cost of event hosting, the travel expenses of invited speakers, material preparation, in-course catering and video recording and production services. The workshop registrations were free of charge although participants had to cover their own travel and lodging.

2.4 Workshop Promotion

The workshops were advertised by sending invitations throughout the HPC community and through coordinated press releases. Announcements and press releases were published at least one month before the hosted events. The Finnish and Swiss workshop press releases were published on the 23rd April 2009. The Polish workshop press release was published on the 17th September 2009. The Spanish workshop press release was published on the 11th August 2009. The workshop announcements were also published on the PRACE HPC-training website[1].

[1] http://www.prace-project.eu/hpc-training

3 Workshop Events

This section presents the workshop details for each of the code-porting events highlighted in Chapter 2.1. The information in this section was contributed by the principal contacts at each workshop site after completion of their event. For simplicity, the workshop details are introduced in chronological order.

3.1 Finnish Workshop on Application Porting and Performance Tuning

Workshop Location and Date

The Finnish workshop was hosted at the HTC Keilaniemi Conference Centre[2] during the 11th-12th June 2009, in Espoo, Finland, close to the CSC facilities[3].

Workshop Theme

The goal of this workshop was to disseminate the valuable information that had been acquired within PRACE WP6, in porting and optimising applications to the PRACE prototype systems. The programme for the workshop therefore focused on a series of technical lectures presenting the porting, optimization and profiling techniques currently employed by PRACE researchers within WP6. These lectures included information on new programming models for petascale computing, numerical libraries and performance measurement tools. In addition, these lectures were complemented by a series of case studies, describing the application of these techniques and technologies on real applications.

Workshop Speakers

The invited speakers for the workshop were predominantly selected from active researchers from within WP6. Table 3 lists the final selection of speakers, their affiliations and brief biographical summaries. Speakers were selected due to their primary involvement in the development of the tool/application/model under study.

Speaker	Country	Brief Biography
Carlo Cavazoni	Italy	Staff member of the CINECA supercomputing group
Jussi Enkovaara	Finland	Application scientist at CSC - IT Center for Science
Olli-Pekka Lehto	Finland	Evaluator of new HPC technologies at CSC-IT Center for Science
Mohammed Jowkar	Spain	Researcher in parallel numerical simulations at the Barcelona Supercomputing Center
Brian Wylie	Germany	Research scientist developing scalable tools at the Juelich Supercomputing Centre
Andy Sunderland	UK	Researcher in the Advanced Research Computing Group at the Daresbury Laboratory
Judit Gimenez	Spain	Performance tools group manager at Barcelona Supercomputing Centre
Manuel Guidon	Switzerland	PhD student in the field of theoretical chemistry at University Zurich, Switzerland

Table 3: Speaker List for Finnish Code-Porting Workshop

The full biographies of the Finnish workshop speakers are given in Annex 5.1.

[2] http://www.htc.fi/
[3] http://www.csc.fi

Workshop Programme

The structure of the two-day workshop was as follows:

Day 1	1. Optimal Usage of Numerical Libraries
	2. Hybrid MPI + OpenMP Programming Model
	3. GPAW Case Study
	4. CP2K Case Study

Day 2	1. Scalasca Performance Measurement Tool
	2. Paraver Tools
	3. Code Saturn Case Study
	4. Porting to the CELL Architecture

The complete programme for the Finnish workshop can be found in Annex 5.2.

Workshop Social Event

The workshop hosted a social event on the evening of the 11th June involving refreshments, dinner and sauna.

Workshop Participants

The final attendance for the workshop was 34 persons, nine of which were invited speakers. The full country breakdown for participants is given in Table 4.

Country	Participants
Finland	23
Spain	4
Germany	3
Switzerland	1
Sweden	1
Italy	1
United Kingdom	1

Table 4: Country Breakdown for Finnish Workshop Participants

Workshop Material and Videos

The workshop slides were immediately made available via the PRACE Training Portal and local CSC webpages. Furthermore, every session was also recorded to digital video allowing the workshop material to be readily available to larger audiences outside the scope of the workshop. The complete slide and video material can be viewed online through the PRACE training portal at the following URL:

http://www.prace-project.eu/hpc-training/prace-code-porting-videos/prace-workshop-on-application-porting-and-performance-tuning

Workshop Photos

The workshop experience was captured on photo by local CSC staff throughout the workshop. A sample of workshop photos is provided below.


Photos: Workshop participants (left) and Dr. Cavazoni during a lecture (right)

3.2 Swiss Workshop on Cray XT5 Code Porting

Workshop Location and Date

The Swiss code-porting workshop was hosted at the Swiss National Supercomputing Centre[4], during the 13th-15th July 2009, in Manno, Switzerland.

Workshop Theme

The focus of this three-day workshop was to provide students with advanced training and expertise in porting application codes to the Cray XT5 architecture; one of the PRACE prototype systems hosted at CSC, Finland[5]. The format of the workshop saw each day comprise of morning lectures in porting and optimization theory for the Cray XT5 followed by afternoon sessions whereby participants could apply their new knowledge to real application codes. Participants were highly encouraged to bring their own applications to the workshop and were equally encouraged to benefit from the Cray Inc. porting and optimization staff that was present.

Workshop Speakers

Cray Inc. kindly supplied the invited speakers for the workshop. The speakers are renowned throughout the HPC community for their expertise in understanding the Cray XT5 architecture and providing porting expertise and developing profiling tools for Cray Inc. clients worldwide. Table 5 lists the speakers, their affiliations and brief biographical summaries.

Speaker	Country	Brief Biography
John Levesque	US	Director, Cray Supercomputing Center of Excellence, Oak Ridge National Lab (ORNL).
Luiz De Rose	US	Director of Programming Environment and Tools, Cray Inc.
Roberto Ansaloni	Italy	Engineer within Benchmark Team, Cray Inc.

Table 5: Speaker List for Swiss Code-Porting Workshop

The full biographies of the workshop speakers are given in Annex 5.3.

[4] http://www.cscs.ch
[5] http://www.csc.fi

Workshop Programme

The structure of the three-day workshop was as follows:

Day 1	1. Architecture of the AMD Quad Core Processor
	2. Compilation and Vectorization on the XT5
	3. Using the CrayPAT Profiling Tool
	4. Code Porting "Hands-On" (I)

Day 2	1. Quad-Core Optimization
	2. Apprentice^2 Profiling Tool
	3. Code Porting "Hands-On" (II)

Day 3	1. XT5 Message-Passing Optimizations
	2. Case Study: CP2K
	3. MPI Performance with Apprentice^2
	4. Code Porting "Hands-On" (III)

The complete programme for the Swiss code-porting workshop can be found in Annex 5.4.

Workshop Social Event

The workshop hosted an aperativo and dinner cruise on the evening of the 14th July on Lake Lugano.

Workshop Participants

The final registration for the workshop included 21 participants.The full country breakdown for participants is given in Table 6.

Country	Participants
Switzerland	14
Italy	2
United States	2
United Kingdom	1
Germany	1
Austria	1

Table 6: Country Breakdown for Swiss Workshop Participants

Workshop Material and Videos

Each registered participant received a handbook at the outset of the workshop containing *all* slide presentations. The workshop slides were also made available via the PRACE Training Portal and CSCS websites. Furthermore, every session was also recorded to digital video allowing the workshop material to be readily available to larger audiences outside the scope of the workshop. The slide and video material can be viewed online through the PRACE training portal at the following URL:

http://www.prace-project.eu/hpc-training/prace-code-porting-videos/training-material-from-prace-cray-xt5-code-porting-workshop-at-csc-switzerland-july-13-15/

3.3 Polish Workshop on NEC SX-9 and BlueGene/P Code Porting

Workshop Location and Date

The Polish workshop was hosted at the Academic Computer Centre[6] CYFRONET AGH during the 14th-16th October 2009, in Cracow, Poland. The workshop was held in association with the Cracow Grid Workshop 2009[7].

Workshop Theme

The goal of this workshop was to provide students with hands-on experience with porting application codes to the BlueGene/P (FZJ, Juelich) and NEC SX-9 (HLRS, Stuttgart) PRACE prototype systems. The first day of the workshop focused on introductory lectures to the prototype systems while the second and third days concentrated solely on "hands-on" code-porting and optimisation exercises. Access to the two prototype machines was divided between morning and afternoon sessions; the morning session focused purely on the BlueGene/P system while the afternoon sessions focused on the NEC SX-9 systems. This approach allowed the students to gain a clearer understanding of the fundamental differences between the two machine architectures.

Workshop Speakers

The invited speakers for the workshop were selected due to their close associations with the BlueGene/P and NEC SX-9 prototype systems. Table 7 lists the speakers, their affiliations and brief biographical summaries.

Speaker	Country	Brief Biography
Lukas Arnold	Germany	Research scientist in the Simulation Laboratory Plasma Physics at the Institute for Advanced Simulation, FZJ, Germany.
Kamil Iskra	U.S.	Assistant Computer Scientist at Argonne National Laboratory
Harald Klimach	Germany	User application support and application benchmarking at High Performance Computing Centre Stuttgart (HLRS)
Radoslaw Januszewski	Poland	Research scientist, Poznan Supercomputing and Networking Centre (PSNC)

Table 7: Speaker List for Polish Workshop

The full biographies of the Polish workshop speakers are given in Annex 5.5.

Workshop Programme

The structure of the three-day workshop was as follows:

Day 1	1. System Software for Petascale and Beyond
	2. Introduction to the IBM BlueGene/P
	3. Introduction to the NEC SX-9
	4. Green Computing

Day 2	1. Code-Porting on BlueGene/P
	2. Code-Porting on NEC SX-9

[6] http://www.cyf-kr.edu.pl/en/
[7] http://www.cyf-kr.edu.pl/cgw09/

Day 3	1. Code-Porting on BlueGene/P
	2. Code-Porting on NEC SX-9

The complete programme for the Polish workshop can be found in Annex 5.6.

Workshop Social Event

The workshop hosted a dinner on the evening of the 15th October at the restaurant of the Hotel Stary.

Workshop Participants

Registration for the workshop was open until October 4th 2009. Registration was conducted online[8]. The maximum number of participants for the event was limited to 50 people. The first day of the workshop was held in association with the Cracow Grid Workshop and attracted close to 200 participants from across the European Union. The "hands-on" sessions, on the second and third days of the workshop, had thirty-39 registered participants, the majority of which were from Poland. The full country breakdown for participants is given in Table 8.

Country	Participants
Poland	35
Germany	3
Ukraine	1

Table 8: Country Breakdown for Polish Workshop Participants

Workshop Material and Videos

The workshop slides were made available via the PRACE Training Portal. Furthermore, every session was also recorded to digital video allowing the workshop material to be readily available to larger audiences outside the scope of the workshop. The slide and video material can be viewed online through the PRACE training portal at the following URL:

http://www.prace-project.eu/hpc-training/prace-code-porting-videos/prace-code-porting-workshop-in-cracow/

Workshop Photos

The workshop experience was captured on photo by staff throughout the workshop. A sample of workshop photos is provided below.



Photos: Workshop participants (left) and guest lecturers (right)

Further photos can be found at http://fivo.cyf-kr.edu.pl/prace/photos.php

[8] http://fivo.cyf-kr.edu.pl/prace

3.4 Spanish Workshop on Cell and GPGPU Code Porting

Workshop Location and Date

The Spanish workshop was hosted at the North Campus, Technical University of Catalonia[9], during the 21st - 23rd October 2009, in Barcelona, Spain.

Workshop Theme

The focus of this workshop was to provide students with advanced training in programming models and optimization techniques for CELL and GPGPU-based systems that comprise some of PRACE's prototype architectures. The first day of the workshop focused on the OpenMP 3.0 programming model. The second day focused on application porting to CELL-based systems. The third and final day focused on UPC, and the CUDA and OpenCL programming models for GPGPU systems.

Workshop Speakers

The invited speakers for the workshop were selected due to their close associations with the advanced programming models and hardware introduced at the workshop. Table 8 lists the speakers, their affiliations and brief biographical summaries.

Speaker	Country	Brief Biography
Montse Farreras	Spain	Associate professor at Universitat Politecnica de Catalunya (UPC) and an associate researcher in the Programming Models Team (Computer Science) at BSC (Barcelona Supercomputing Center).
Marc Gonzalez	Spain	Associate Researcher, Department of Computer Science, Barcelona Supercomputing Centre (BSC)
Massimiliano Fatica	U.S.	Senior Applied Engineer, NVIDIA
Jordi Caubet	Spain	IT Specialist, IBM, Spain
Rosa M. Badia	Spain	Scientific Researcher for CSIC and manager for Grid Computing and Cluster Research Group, Barcelona Supercomputing Centre

Table 9: Speaker List for Spanish Workshop

The full biographies of the Spanish workshop speakers are given in Annex 5.7.

Workshop Programme

The structure of the three-day workshop was as follows:

Day 1	1. OpenMP 3.0 Programming
Day 2	2. Programming the CELL
Day 3	1. UPC Programming
	2. CUDA Programming
	3. OpenCL Programming

The complete programme for the Spanish workshop can be found in Annex 5.8.

Workshop Social Event

The workshop hosted a dinner on the evening of the 22nd October at a restaurant in Barcelona.

[9] http://www.upc.edu/eng

Workshop Participants

The final registration for the workshop included 33 participants, including speakers, with the majority of the participants attending from within Spain. The full country breakdown for participants is given in Table 9.

Country	Participants
Spain	29
Ireland	1
Serbia	1
United Kingdom	1
United States	1

Table 10: Country Breakdown for Spanish Workshop Participants

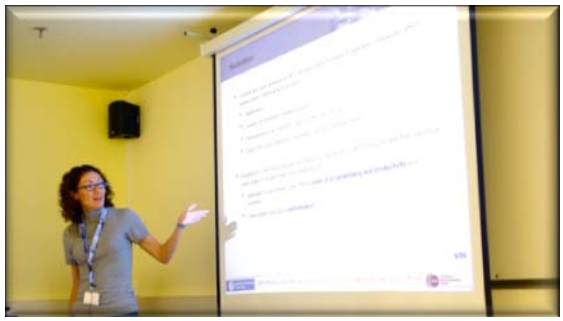
Workshop Material and Videos

The workshop slides were made available via the PRACE Training Portal. Furthermore, every session was also recorded to digital video allowing the workshop material to be readily available to larger audiences outside the scope of the workshop. The slide and video material can be viewed online through the PRACE training portal at the following URL:

http://www.prace-project.eu/hpc-training/prace-code-porting-videos/prace-code-porting-workshop-in-barcelona/

Workshop Photos

The workshop experience was captured on photo by staff throughout the event. A sample of workshop photos is provided below.

Photos: Workshop participants (left) and Dr. Farreras during a presentation (right)

4 Conclusions from the Code-Porting Workshops

The hosting of code-porting and scaling workshops are valuable opportunities for participants to acquire the necessary skills and techniques that will be required to adapt user applications to the leadership class systems that are envisaged as part of the PRACE computing research infrastructure and subsequently accelerate their scientific output on both national and international levels. Without advance experience with the machine architectures and programming paradigms that will be required by these Tier-0 systems, users will not be in a position to effectively exploit the architectures as and when they become available for mainstream scientific use. It is hoped this series of workshops is a significant step towards providing this knowledge and experience to future PRACE infrastructure users.

Through local as well as collective planning, four successful code-porting and scaling workshops were organized by the PRACE partners of Finland, Switzerland, Spain and Poland geographically spanning the breadth of Europe and welcoming over 100 participants. On completion of all the workshops, each hosting site remained within their budget of eight thousand Euros and no additional funding was required during the preparation of the individual events.

The workshops also successfully targeted a diverse range of PRACE prototype platforms, including the Cray XT5, IBM BlueGene/P, NEC SX-9 and IBM Cell clusters. Furthermore, participants gained valuable insight into the programming models and software techniques required to exploit efficiently these high-performance systems. In many cases participants received face-to-face support from some of the world's foremost porting experts, in adapting their own codes to the prototype systems.

A sustained advertising campaign, featuring press releases, invitations and announcements ensured that the workshops were adequately promoted in advance of the registration deadlines, and attracted over 100 participants from both Europe and the rest of the World.

One of the most successful outcomes of the workshops was the large collection of training material that is now freely available from within the PRACE training portal. In particular over 46 hours of video content was captured to ensure that the HPC community at large, are able to benefit from the expert instruction and knowledge transfer, on demand and at no cost.

Across all workshops, the feedback was positive and many participants welcomed the opportunity to gain first-hand instruction, by leading experts, on adapting their codes to the next generation of high-performance computing hardware.

From an organisational viewpoint, it must be noted that future workshops need to ensure that that communication between speakers is satisfactory enough to prevent duplication of material within and between workshops. Furthermore, workshop organisers should insist that "hands-on" code porting and scaling sessions feature significantly within their programmes to justify these funded events. With growing experience, future workshops will begin to strike the delicate balance between lectures and "hands-on" sessions to ensure the participants maximise the knowledge and experience they acquire through these events.

It is clear that this initial series of code-porting workshops was a huge success from the perspective of the instructors, participants and the HPC community who can also benefit from the wealth of knowledge that is now freely available in both slide and video formats. It is sincerely hoped that this trend can continue to be realised through forthcoming PRACE Training and Education events.

5 Annex

5.1 Finnish Workshop Speakers (Full Biographies)

Mohammad Jowkar
Received his M.Sc. in Computer Science from University of Copenhagen, Denmark in 2007. His thesis work was regarding the Cell processor and High Performance Computing, for which he received the 2007 'Best Master's Thesis' award by the 'Danish Computer Science Society'. Today he is a researcher in parallel numerical simulations at the Barcelona Supercomputing Center where he is completing his PhD. Mohammad's PRACE activities are mainly in WP6, where he is the task leader of Task 6.4 (Petascaling of Applications).

Brian Wylie
Received his PhD in computational physics from the University of Edinburgh, Scotland in 1991. He worked at EPCC (Edinburgh), CSCS (Manno), the University of Wisconsin (Madison) and Sun Microsystems (Menlo Park) prior to joining FZJ (Juelich) in 2004 as a research scientist developing scalable tools for parallel performance analysis.

Andrew Sunderland
Received his doctorate in Computational Science from the University of Liverpool in 2000. He has worked at the Institute for Advanced Scientific Computation at the University of Liverpool, and more recently, the Advanced Research Computing Group at the Daresbury Laboratory of the Science and Technology Facilities Council in the UK. His PRACE activities have focused on application code porting, optimization and analysis in WP6.

Judit Gimenez
Received her degree in Computer Science in 1989 from the Universitat Politecnica de Catalunya. After working on different areas that include technology transfer and user support, she started to work on performance tools in year 2000, being currently the performance tools group manager of BSC (Spain).

Olli-Pekka Lehto
Has a Master's Degree in networking technology from the Helsinki University of Technology. He joined CSC - IT Center for Science in 1998 and currently specializes in evaluating new HPC technologies. In PRACE, Olli-Pekka is involved in many of the benchmarking activities (WP5-8).

Jussi Enkovaara
Received Diploma in Computational Physics in 1999 and Ph.D in Computational Physics in 2003 from Helsinki University of Technology, Finland. Worked as post-doctoral researcher at FZJ (Juelich), Germany in 2003-2005. From 2005 on has worked as application scientist at CSC - IT center for science, Finland. PRACE activities are in optimization and petascaling (WP6), BCO of GPAW.

Dr. Carlo Cavazzoni
Graduated in physics at the University of Modena in 1994 (with mark 110 / 110 cum laude), and subsequently he has attained the degree of Doctor Philosopiæ at the International School for Advanced Studies (ISAS-SISSA) of Trieste in 1998 (with mark 30 / 30 cum laude, thesis title: "Large Scale First-Principles Simulations of Water and Ammonia at High Pressure and Temperature"). He is presently a staff member of the CINECA supercomputing group. During his Ph.D., he has studied various problems concerning the implementation and the efficiency of parallel numerical algorithms being used in physical computer simulations. He is familiar

with many supercomputers environment and he has a good knowledge of many computer languages (FORTRAN77, FORTRAN90, C, C++) and of software engineering techniques. In the PRACE project Carlo Cavazzoni is mainly involved in activities of WP6.

Manuel Guidon
Received his Diploma in Computational Physics in 2005 from ETH Zuerich, Switzerland. Since then he is working as a PhD student in the field of theoretical chemistry at University Zurich, Switzerland at the Institute of Physical Chemistry. His PRACE activities are mainly the machine (WP7), i.e. CRAY-XT5.

5.2 Finnish Code-Porting Workshop (Complete Programme)

Day One - Thursday, 11 June 2009	
08:45 - 09:00	Welcome
09:00 - 10:30	**Olli-Pekka Lehto:** Numerical Libraries
10.30 – 10.45	Coffee Break
10:45 - 12:15	**Jussi Enkovaara:** Case study (GPAW)
12:15 – 13:00	Lunch
13:00 – 14.30	**Carlo Cavazzoni:** Hybrid programming with MPI & OpenMP
14.30 – 14.45	Coffee
14.45 – 15.30	**Manuel Guidon:** Case study (CP2K)
16.30 -	**Social Event:** Sauna, Dinner and Refreshments
Day Two - Friday, 12 June 2009	
09:00 – 10.30	**Brian Wylie:** Scalasca Performance Tool
10:30 – 10.45	Coffee
10.45 – 12.15	**Judit Gimenez:** Paraver Performance Tool
12:15 – 13:00	Lunch
13:00 – 14.30	**Mohammad Jowkar:** Porting to the CELL
14.30 – 14.45	Coffee
14.45 – 15.30	**Andrew Sunderland:** Case study (Code-Saturn)

5.3 Swiss Workshop Speakers (Full Biographies)

John Levesque
Director of the Cray Supercomputing Center of Excellence at the Department of Energy's Oak Ridge National Laboratory (ORNL), the world's most powerful supercomputer for open (non-classified) scientific research. Levesque leads a team of engineers providing application and high performance computing expertise to researchers using ORNL systems. From 2001 to 2003, Levesque was a senior principal engineer responsible for the benchmarking initiatives for the Cray XI system, playing a key role in helping CINECA, Italy's national supercomputer center and the Department of Defense Modernization Program optimize their applications. Prior to Cray, Levesque was the director of the Advanced Computer Technology Center at IBM's Watson Research Center where his team received the Scientific Achievement Award for contributing more than $200 million in new business sales in 2000.

Dr. Luiz DeRose
Ph.D. in Computer Science from the University of Illinois at Urbana-Champaign. He is the

Programming Environments Director and a Senior Principal Engineer at Cray, Inc., where he is responsible for the programming environment strategy for all Cray systems. Before joining

Cray in 2004, Dr. DeRose was a research staff member at IBM Research where he focused his efforts on designing and developing application performance tools for high performance computing systems. Dr. DeRose has more than 20 years of experience in HPC, working in the area of software support for high performance computation. He was responsible for the design and development of performance tools, such as FALCON, SIGMA, the HPM Toolkit, the CrayPat Performance Collector and the Cray Apprentice2 Performance Analyzer. With a deep knowledge of the HPC programming environment, over the span of his career Dr. DeRose has published more than 40 peer-review articles in scientific publications, primarily on the topic of compilers and performance tools.

5.4 Swiss Code-Porting Workshop (Complete Programme)

Day One - Monday, 13th July 2009	
09:00 - 09:30	Registration
09:30 - 10:30	**John Levesque:** Architecture of the AMD Quad-Core
10:30 – 10.45	Break
10:45 - 11:30	**John Levesque:** Compiler Considerations on Quad-core
11.30 – 12:15	**Luiz DeRose:** Using CrayPAT to Profile on XT5
12:15 – 14:00	Lunch
14:00 – 16:30	Hands-On(I)
Day Two - Tuesday, 14th July 2009	
09:00 - 10:30	**John Levesque:** AMD Quad-core Optimizations
10:30 - 10:45	Break
10:45 - 11:45	**Luiz DeRose:** Apprentice^2
11:45 - 13:30	Lunch
13:30 - 16:30	Hands-On(II)
19:30 -	Dinner
Day Three - Wednesday, 15th July 2009	
09:00 - 10:30	**John Levesque:** Message-Passing Optimizations
10:30 - 10:45	Break
10:45 - 11:45	**Joost VandeVondele:** Case Study: CP2K
11:45 - 12:45	**Luiz DeRose:** MPI Performance with Apprentice^2
12:45 - 14:30	Lunch
14:30 - 16:00	Hands-On(III)
16:00 -	Farewell

5.5 Polish Workshop Speakers (Full Biographies)

Lukas Arnold

Received his Diploma in Computational Physics in 2005 and PhD in theoretical Plasma Physics from Ruhr-University Bochum, Germany in 2009. Since then he is a research scientist in the Simulation Laboratory Plasma Physics at the Institute for Advanced Simulation, FZJ, Germany. His PRACE activities are mainly the machine (WP5) and application (WP6) benchmarking as well as the compilation of the PRACE application benchmark suite.

Kamil Iskra

Received his M.S. in computer science from AGH University of Science and Technology in Cracow, Poland in 1999. In 1999-2000 he was a scientific programmer at the University of Amsterdam, Netherlands, where he worked on task migration for parallel applications. He got his Ph.D. in computer science from the University of Amsterdam in 2005, in the area of

parallel discrete event simulation. In 2005 he joined Argonne National Laboratory in the US, first as a postdoctoral researcher, and, since 2008, as an assistant computer scientist. He works on operating systems and I/O forwarding infrastructure for massively parallel machines.

Harald Klimach

Received a Diploma in 2005 from University of Stuttgart. Since then he is working in DEISA in a Joint Research Activity on coupled computations, by now working in user application support and application benchmarking. Helped in building the HLRS Fortran Course. Since January 2008 also working in PRACE, mainly on application benchmarks.

5.6 Polish Code-Porting Workshop (Complete Programme)

Day One - Wednesday, 14 October 2009	
08:00 - 08:30	Registration *(for 1st day attendees)*
10:30 - 11:15	**CGW09 - Keynote**
	Kamil Iskra: System Software for Petascale and Beyond
14:00 - 15:30	**CGW09 - Session C6**
	Lukas Arnold: Introduction to the IBM BlueGene/P Installation at the Forschungszentrum Julich
	Harald Klimach: NEC SX installation at High Performance Computing Center Stuttgart and its applications
	Radoslaw Januszewski: Green computing in practice. Cons and pros of modern system architectures.
Day Two - Thursday, 15 October 2009	
09:00 - 09:30	Registration
09:30 - 11:00	**Lukas Arnold:** Code porting on BlueGene/P
11:00 - 11:15	Coffee break
11:15 - 12:45	**Lukas Arnold:** Code porting on BlueGene/P
12:45 - 14:00	Lunch break
14:00 - 15:30	**Harald Klimach:** Code porting on NEC SX-9
15:30 - 15:45	Coffee break
15:45 - 17:15	**Harald Klimach:** Code porting on NEC SX-9
20:00 - 22:00	Dinner
Day Three - Friday, 16 October 2009	
09:30 - 11:00	**Lukas Arnold:** Code porting on BlueGene/P
11:00 - 11:15	Coffee break
11:15 - 13:00	**Lukas Arnold:** Code porting on BlueGene/P
13:00 - 14:00	Lunch break
14:00 - 15:30	**Harald Klimach:** Code porting on NEC SX-9
15:30 - 15:45	Coffee break
15:45 - 17:15	**Harald Klimach:** Code porting on NEC SX-9
17:15 - 17:30	Good bye

5.7 Spanish Workshop Speakers (Full Biographies)

Montse Farreras

Received her MSc and PhD degrees in computer science at the Computer Architecture Department in UPC (Universitat Politecnica de Catalunya) in Barcelona in 2002 and 2008, respectively. She works as an associate professor at the same University, and an associate researcher in the Programming Models Team (Computer Science) at BSC (Barcelona

Supercomputing Center). She has been collaborating with the Programming Models and Tools for Scalable Systems group at IBM Research since 2004, working on a scalable Runtime System for the XLUPC compiler. Her research interests are in programming models and languages for large scalable systems.

Marc Gonzàlez

Received the Engineering degree in Computer Science in 1996 and the Computer Science PhD degree on December 2003. His research has been developed around parallel programming models and high performance computing, in particular, the OpenMP programming model. His current research is centred on this programming model and its use on heterogeneous architectures, based on accelerators and local memories. The main research activities are the design and implementation of software cache techniques for the IBM Cell BE processor as well as the implementation of runtime libraries and compiler support for the OpenMP programming model on this architecture.

Massimiliano Fatica

Received a Laurea in Aeronautical Engineering in 1991 and a PhD in Theoretical and Applied Mechanics in 1995, both from the University of Rome "La Sapienza". He is a Senior Applied Engineer at NVIDIA where he works in the area of GPU computing (high-performance computing and clusters). Prior to joining NVIDIA in 2006, he was a research staff member at Stanford University in the Center for Turbulence Research, where he worked on Large Eddy Simulation and CFD applications for the Stanford Streaming Supercomputer.

Jordi Caubet

IT specialist for IBM in Barcelona (Spain). His areas of expertise include High Performance Computing, IBM System p and BladeCenter servers including new Cell/B.E. technologies and Linux operating systems. He holds a degree in computer science from Technical University of Catalonia (Barcelona) and has been working in the IT industry for 10 years. He works on the IBM Innovation Initiative at the Barcelona Supercomputing Center (BSC-CNS) collaboration agreement.

Rosa M. Badia

PhD on Computer Science (1994) from the Technical University of Catalonia (UPC). Since year 2008 she is a Scientific Researcher from the Consejo Superior de Investigaciones Científicas (CSIC) and manager of the Grid Computing and Cluster research group at the Barcelona Supercomputing Center (BSC). She has been involved in teaching and research activities at the UPC since 1989 to 2008, where she has been an Associated Professor since year 1997. From 1999 to 2005 she has been involved in research and development activities at the European Center of Parallelism of Barcelona (CEPBA). Her current research interest are: performance prediction and modeling of MPI programs and programming models for complex platforms (from multicore to the Grid/Cloud). She has participated in several European projects and she is currently participating in projects BEinGRID, Brein, XtreemOS and OGF-Europe and it is a member of HiPEAC2 NoE. She has collaborated with PRACE in the definition of benchmarks and its porting to StarSs.

5.8 Spanish Code-Porting Workshop – Complete Programme

Day One - Wednesday, 21st October 2009	
09:30 - 10:00	Registration
10:00 - 10:15	Welcome
10:15 – 10.45	**Jordi Caubet:** Introduction to Parallel Programming
10:45 - 11:30	**Jordi Caubet:** OpenMP Basics
11.30 – 12:00	Break
12:00 – 12:15	**Jordi Caubet:** Synchronization Basics
12:15 – 13:00	Hands-On(I)
13:00 – 14:00	Lunch
14:00 – 14:30	**Jordi Caubet:** Task Parallelism in OpenMP
14:30 – 15:15	Hands-On(II)
15:15 – 15:45	**Jordi Caubet:** Data Parallelism in OpenMP
15:45 – 16:15	Break
16:15 – 17:00	Hands-On (III)
17:00 – 17:30	**Jordi Caubet:** Other OpenMP topics
17:30 – 18:00	**Jordi Caubet:** The Future of OpenMP
18:00 -	Visit to MareNostrum Supercomputer (Optional)
Day Two - Thursday, 22nd October 2009	
09:30 - 10:45	**Jordi Caubet:** Introduction to CELL and SDK
10:45 - 11:15	**Marc González:** OpenMP on CELL BE
11:15 - 11:30	Coffee break
11:30 - 13:30	**Rosa Badia:** CELL Programming (StarSs)
13:30 - 14:30	Lunch
14:30 - 16:00	**Jordi Caubet:** CELL Programming Hands-On(I)
16:00 - 16:15	Coffee break
16:15 - 17:30	**Jordi Caubet:** CELL Programming Hands-On(II)
21:00 -	Dinner
Day Three - Friday, 23rd October 2009	
09:30 - 11:00	**Montse Ferraras:** UPC Theory
11:00 - 11:15	Coffee break
11:15 - 13:00	**Montse Ferraras:** UPC Hands-On
13:00 - 14:00	Lunch break
14:00 - 16:00	**Massimiliano Fatica:** Introduction to CUDA
16:00 - 16:15	Coffee break
16:15 - 18:00	**Massimiliano Fatica:** CUDA and OpenCL
18:00 -	Farewell