

NEWSletter

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Advanced tools to design future jet engines

Pirjo Rötökönen

Increasingly stringent requirements for energy efficiency and noise reduction in jet engines are tightening the screw in their development and design. Cenaero, an applied research centre for modelling and numerical simulation, is developing new methods that will help in designing high-performance jet engines. Cenaero was granted access to PRACE resources in PRACE Preparatory Access for an industrial pilot project “noFUDGE”. Previously Cenaero has been granted access in the DECI (Distributed European Computing Initiative) call.

For a long time one of the main problems in applied fluid mechanics – especially in industrial flows – has been the estimation of the impact of turbulence.

“Up to now aircraft and engine manufacturers have been using mostly time-averaged computational methods, in combination with lower accuracy discretisation techniques, for their design purposes. These algorithms will continue to be used, at least for a while, but they need to be complemented with more advanced computational tools. First of all, these methods are simply not applicable for some types of flows. An important application is the prediction of noise, for example generated by a flow from propellers or flow instabilities in compressors and fans. By applying larger computing resources we can directly simulate part of the turbulence,” explains

Koen Hillewaert, Argo Team Leader at the Cenaero research centre in Belgium.

“For low speeds or small geometries the size of the turbulence is such that we cannot even get an accurate value of the time-averaged forces and performance if we do not compute part of the turbulent structures directly. These conditions are prevalent for instance on part of wind turbine blades and in some parts of a jet engine,” he adds.

Industrial applications in mind

Cenaero’s aim is to provide a numerical algorithm based on the Discontinuous Galerkin Method (DGM), to be used for computations with full (DNS or Direct Numerical Simulation) and partial (LES or Large Eddy Simulation) resolution of turbulence in wall-bounded flows, especially in turbomachines.

“We are convinced that DGM combines the high order of accuracy that is currently offered by academic codes to the geometric flexibility characteristic of industrial codes, and at the same time provides computational efficiency and parallelisability. This high order of accuracy is indispensable to represent turbulent structures adequately, but is not provided by state-of-the-art industrial codes. At Cenaero, we are primarily interested in the industrial application. The academic aspect – although also very important as some of the numerical technology still needs to be developed – is a secondary goal.”

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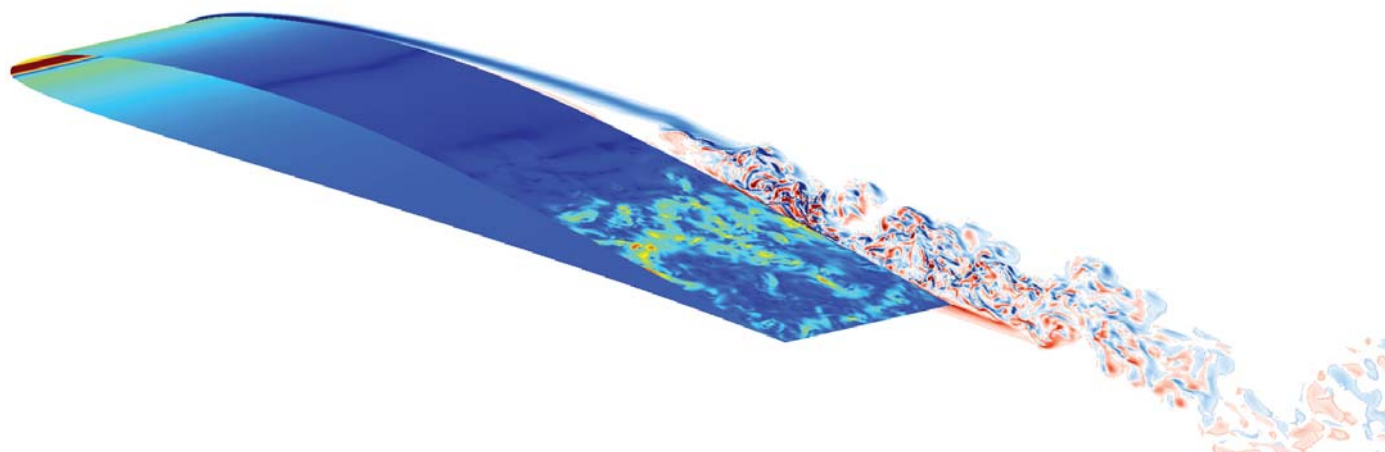
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“We will be able to use our method in the context where the turbulence occurs very close to walls, where there is more complexity to take into account – you simply have larger demands for resolution there. The turbulence is influenced by the walls in the flows that interest us, because we focus on turbomachinery, jet engines and propellers.”



DNS computations of the transitional flow around the Eppler E387 airfoil during the DECI project “Cobauld” – computed isocontours of vorticity on the spanwise periodic plane and skin friction on the airfoil surface. © Cenaero

Huge computational resources

For the turbulence computations performed by the research team at Cenaero, huge computational resources are needed.

"That is why we turned to the world-class supercomputers of DECI (Distributed European Computing Initiative). With these resources we could provide a proof-of-concept of the method focused on full resolution of the turbulence, by performing the direct simulation of the transitional flow around a low-speed airfoil. DECI also gave us access to machines that have different architecture from what we usually have at computational centres. It was a unique opportunity to test if the code would work satisfactorily in this kind of architecture. Furthermore we were attracted by the support from specialists in porting and optimizing the code," Hillewaert says.

"To show that the method is viable, we compared it to experimental results and DNS computations with a conventional low-order discretisation. It was clear that the computations really correspond to what was measured, and that the method really offers a huge advantage with respect to the standard discretisation method, as it allowed us to capture the real physics rather than a result that only looks acceptable. DGM moreover offers us a visual means to assess mesh resolution."

The promising results of this project lay the ground for further development using the supercomputing resources of PRACE. Cenaero

was granted 2 000 000 core-hours on the JUGENE supercomputer in PRACE Preparatory Access call. A first project "noFUDGE" has just been finished, and concerns the transitional flow on a section of low-pressure jet engine turbine blade.

"We are moving towards the resolution of more complex flows and flow conditions that are rather ambitious, leveraging both on the availability of ever more powerful computational resources and the further development of the numerical algorithms."

Convincing the industrial partners

The results achieved in these computations are part of a roadmap towards industrial use of DNS and LES.

"We are showing that with the discontinuous Galerkin method well-resolved computations are feasible, and will give more accurate results, not only for the prediction of noise generation or flow instabilities, but for some cases also in terms of global time-average performance."

"The computations have helped us to convince our industrial partners that we will be able to provide the technology for the computations they would like to do within a few years. These cover essentially broadband and tonal noise generation by fans and open rotors, as well as flow instabilities in turboreactors, such as rotating stall."

These types of computation will be needed

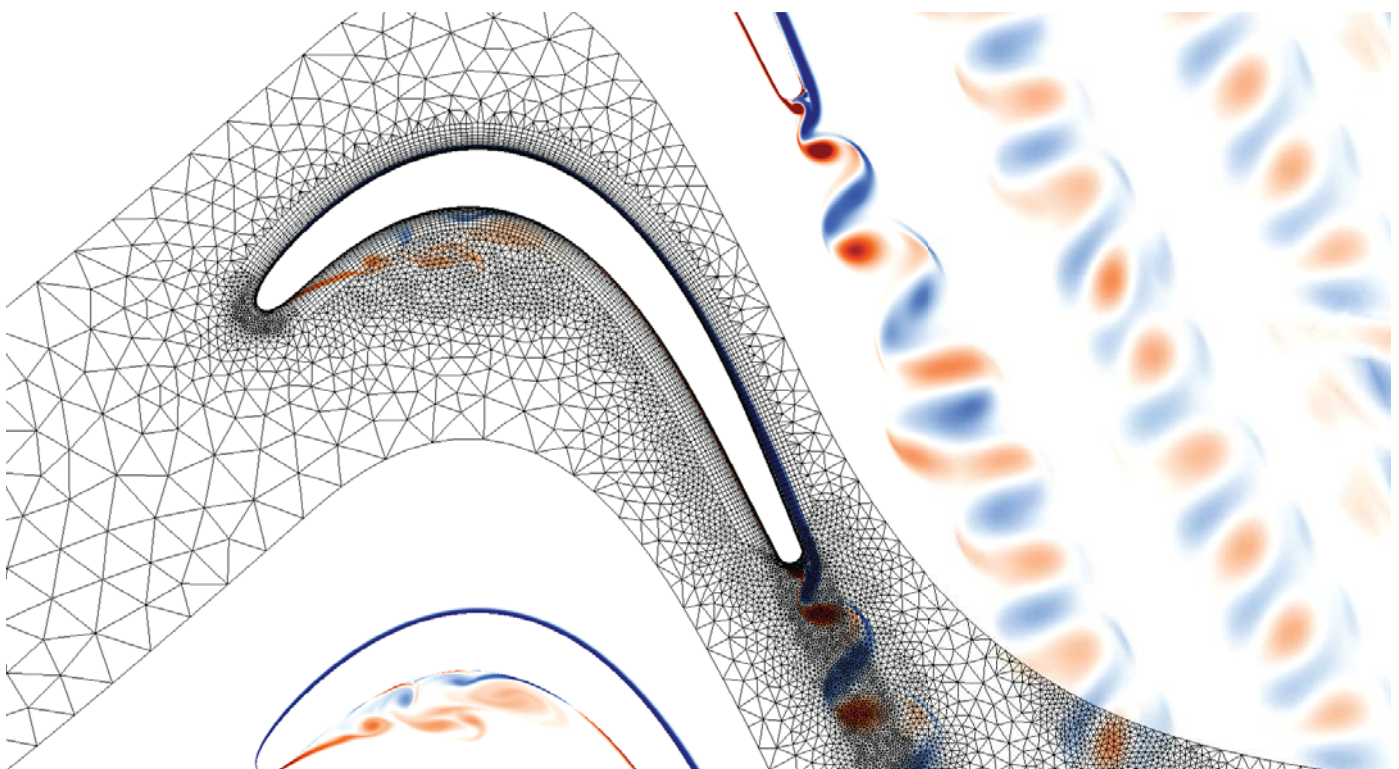


Cenaero Argo Team Leader
Koen Hillewaert © Cenaero

if jet engine industry is to meet the more stringent requirements and regulations in terms of energy efficiency and noise. To keep their competitive edge, manufacturers need to invest in new computational technology now.

"If manufacturers do not provide high efficiency and low noise engines, they will be unable to sell them in the future," Hillewaert points out.

"Clearly the evolution of computation techniques goes hand in hand with the availability of computers. On the one hand as more and more powerful computers are available, we can do more complex computations. On the other hand computational technology has to evolve as more direct resolution of the turbulence becomes feasible and large scale resources need to be used efficiently."



DNS of the transitional flow around a LP turbine blade at $Re=88000$ computed during the PRACE project "noFUDGE" – vorticity isocontours on the spanwise periodic plane and skin friction on the blade surface. © Cenaero

Meeting the PRACE Managing Director

Laetitia Baudin

The PRACE Research Infrastructure appointed Dr. Maria Ramalho as Managing Director of the Association with office in Brussels, Belgium. Maria Ramalho is an expert in the field of telecommunication networks and a skilled project coordinator.

As PRACE Managing Director, what are your main objectives for the PRACE Research Infrastructure (RI)?

We are living historical moments in Europe in terms of the deployment of research infrastructure on high performance computing (HPC). I have been appointed Chair of the Board of Directors (BoD) of the PRACE association in Brussels in June this year and became, thus, the first staff member of PRACE soon after that. This does not mean that I am the sole executive staffed to be blamed or cheered for the achievements of PRACE RI: a Board of 5 Directors preceded my appointment since the creation of the PRACE association back in June 2010! This Board fulfilled successfully the mandate to implement the first calls for proposals and to execute the actions defined by the PRACE Council.

My main objectives are twofold:

- to give the researchers a predominant role in counseling PRACE governance bodies (e.g. Board of Directors, Scientific Steering Committee and Council) in terms of the definition of the PRACE RI services and the expected quality of the service. To this end, the meeting to elect the Chair and members of the User Forum will take place on the 1st of December 2011 in Brussels. The User Forum has an advisory role towards the Association and is to be governed independently from the Association's main bodies.

- to provide visibility to the HPC resources and know-how provided by the different members of PRACE RI. This in order to facilitate the periodic renewal of investments on high performance computing by the member countries of the Association. At the moment, there are 4 countries providing high performance computing resources (France with GENCI, Germany with the GCS, Italy with CINECA and Spain with BSC) to PRACE RI. However, know-how on HPC exists in many others as it can be demonstrated by the PRACE RI offer in terms of training courses, thematic workshops, market surveying, benchmarking and also the identi-

fication of several conferences that are sponsored on HPC related themes in Europe.

The human capital of the Association I composed of over 200 collaborators working in a distributed way all over Europe within the work plan of the co-called PRACE-Implementation Phase projects. The aim of these projects is to transfer 'best-practice' to PRACE RI for the implementation of production services of the PRACE Research Infrastructure. They constitute a complex beehive that is meant to be as transparent as possible towards the actual users of the HPC infrastructure. The Scientific Steering Committee is precisely the Asso-



Dr. Maria Ramalho was appointed as the Managing Director of the PRACE Research Infrastructure. © BSC

ciation's governance body that alerts and proposes the strategic roadmaps of the Association translating the recommendations defined by the User Forum.

What are your first priorities in the three years?

My first priority is to define a strategic roadmap for the bouquet of services that are on offer, in production mode, to the researchers and members of the PRACE RI. The strategic roadmap includes as a key action item, the definition of programmes of access that will address the requirements of research users both from scientific and from engineering

backgrounds. My second priority is to make sure that the contribution of resources (technology and expertise) from the different member countries of the PRACE RI is accounted in fair terms. The aim is to guarantee that the highest ranked Grand Challenges are not rejected access to the HPC facilities due to geographic, institutional or administrative boundaries. My third priority is to define a business model that enables the Association to transit from the current statutes to those of an International organization under European law.

The development of the PRACE AISBL is supported by FP7 funded projects that prepared its creation (PRACE-PP) and now support and accelerate its implementation (PRACE-1IP, PRACE-2IP). How is the AISBL benefiting from the projects?

I would like to recall that the creation of a new entity such as PRACE is not completed by the definition of its legal terms of reference and governance bodies: it still needs to build in the human fabric! This fabric is the most delicate and it must be threaded with the excellent capabilities of each of its collaborators. I always like to emphasize that what is in stake for the next three years is not to work in a project minded way (by definition having a limited fixed term and resources) but to create the solid bricks with each the Association will build itself in the near future. The bricks are the excellent collaborations that are created in the Implementation phase projects and that need to be solidified via Service Level Agreements between the Association and the interested parties.



www.prace-ri.eu

PRACE grants 812 million compute hours on Tier-0 and Tier-1 systems, new call open

PRACE grants 721 million compute hours on Tier-0 systems to 24 research projects in the PRACE 3rd regular call, and 91 million compute hours on Tier-1 systems to 35 projects in the latest DECI (Distributed European Computing Initiative) call.

A total of 53 applications requesting 1.687 million compute core hours were received in the PRACE 3rd regular call, for one year resource allocations on the PRACE Research Infrastructure. 24 of these applications were granted 721 million compute hours on Tier-0 systems. The projects were chosen for their high level of scientific and technical maturity, expected impact, and demonstrated need for Tier-0 resources.

The projects are from the following scientific areas: astrophysics, chemistry and material science,

medicine and life sciences, engineering and energy, fundamental physics and mathematics.

Allocations for Tier-1

54 proposals were received in the latest DECI call, and 35 of these were awarded 91 million processor core hours in total. The call was oversubscribed by more than a factor of 2.5. Due to the excellent quality of the proposals, the contributing partners increased the resources offered to the call by 11% over the original commitment; however this still meant that many good projects could not be granted resources.

New call open

PRACE opened the PRACE 4th regular call for Tier-0 resources and DECI-8 call for Tier-1 resources on 2nd of November, 2011. The call will close on 10th of January, 2012.

This call is the fourth PRACE-RI Regular

call for Project access, inviting applications for high-end (Tier-0) computing resources to carry out projects which have high scientific quality and impact. Allocation will be for one year starting from 1st of May 2012.

The call also invites proposals for project access to Tier-1 resources, via DECI, providing single project cross-national access to national (Tier-1) HPC-resources.

More information about the new call:

www.prace-ri.eu/PRACE-Project-Access-4th-call-for-proposals

Information about awarded projects:

www.prace-ri.eu/hpc-access and www.prace-ri.eu/DECI-7th-Regular-Call

PRACE at SC'11



The PRACE booth at SC'11 attracted numerous visitors. © PRACE

PRACE took part to SC'11 in Seattle, WA, on 14-17 November, 2011.

PRACE Council Chair, Prof. **Achim Bachem** (FZJ, Germany) gave a keynote speech entitled "*PRACE 2020 - a vision for a sustainable European HPC infrastructure*".

PRACE also organised a BoF session entitled "PRACE – The European HPC Infrastructure". In this BoF, PRACE Project Manager, Dr. **Thomas Eickermann** (FZJ, Germany) gave a presentation entitled "*Experiences and perspectives after one year of PRACE Operation*". A PRACE user's point of view was given by Ph.D., Research Group Leader **Mariano Vázquez** (BSC, Spain) in a presentation entitled: "*High Performance Computational Biomechanics and PRACE: The perfect marriage.*"

PRACE was again successfully presenting its achievements in the SC'11 exhibition. The PRACE treasure hunt winner this year was **Aaron Thomas** from Lawrence Berkeley National Laboratory, USA.

Presentations from SC'11 are available at: www.prace-ri.eu/Presentations-at-events



PRACE Council Chair, Prof. Achim Bachem gave a keynote speech at SC'11. © PRACE

Featured PRACE events

Fourth PRACE Executive Industrial Seminar "HPC driving innovation in Europe" Bologna, Italy, 16-17 April 2012

This seminar is designed for strategic decision makers (CIOs, CTOs and R&D Directors) responsible for the design, deployment and operation of computing and data management infrastructures or using them to drive innovation in their enterprises.

The main objective of the seminar is to show how high performance computing

(HPC) and its continuous evolution can enhance European industrial competitiveness, the innovation capabilities it brings to industry and how PRACE can facilitate effective use and development of HPC in Europe.

The programme will focus on successful applications of HPC technologies across a wide spectrum of industries, the pilot usage of PRACE resources in industrial projects and the trends in the evolution of HPC technology. Speakers will include specialists from leading innovative European companies,

HPC experts from academia, as well as representatives of PRACE and the European Commission.

A special emphasis will be placed on how PRACE can facilitate the acquisition of HPC expertise by European industry. In particular, the seminar will endeavour to identify and eliminate barriers to accessing PRACE's expertise by SMEs.

More information at: www.prace-ri.eu



PRACE Winter School CINECA, Casalecchio di Reno (Bologna) Italy, 6-11 February 2012

The PRACE Winter School is an intense, 5 day, graduate level course in high performance computing.

The school will focus on hybrid programming for the best exploitation of massively parallel architectures. The system available at CINECA supercomputing center for hands-on

training is called PLX and is the largest public GPU cluster in Europe. It is made of 274 compute nodes, each containing 2 NVIDIA® Tesla® M2070 and 2 Intel(R) Xeon(R) Westmere six-core E5645 processors.

The school will be held on 6-11 February and the official language of the school is English.

The school is aimed at PRACE users, final year master students, Ph.D. students, and young researchers in computational sciences and engineering, with different backgrounds, interested in applying the emerging technologies on high performance computing to their research.

The school will cover the following topics:

- Massively parallel architectures: BlueGene, hybrid clusters
- Accelerators (NVIDIA GPU, Intel MIC)
- Advanced MPI
- Hybrid programming with OpenMP

- Hybrid programming with CUDA
- Towards new hybrid solutions with MPI
- Some use cases will also be presented.

The number of participants is limited to 40 students. Applicants will be selected according to their experience and qualifications. Knowledge of a high level programming language (C/C++ or FORTRAN) is required, as well as a working experience in parallel programming with MPI.

Attendance is free of charge. Grants are available for participants not funded by their institution and not coming from the Bologna area. Each student will be granted access to CINECA's supercomputing resources for a period of two month after the class.

More information and information about registration at: www.prace-ri.eu

Application deadline: 15 January, 2012

The list of admitted applicants will be published on 25 January, 2012

PRACE Day Hamburg, Germany 17 June, 2012 (in conjunction with ISC'12)

PRACE organises the first PRACE Day in conjunction with the ISC'12 event. The event is a continuum to the successful DEISA PRACE Symposia series.

The PRACE Day takes place at the Radisson Blu Hotel Hamburg.

More information will be available at:

www.prace-ri.eu



Featured project: Mont-Blanc – Europe invests in designing a new energy-efficient Exascale machine



The Mont-Blanc project brings together a purely European consortium gathering industrial technology providers and supercomputing research centres.

Energy efficiency is already a primary concern for the design of any computer system and it is unanimously recognized that future Exascale systems will be strongly constrained by their power consumption. This is why the Mont-Blanc project, which was launched on 14th October in Barcelona with a kick-off meeting, has set itself the following objective: to design a new type of computer architecture capable of setting future global High Performance Computing (HPC) standards that will deliver Exascale performance while using 15 to 30 times less energy.

This new project is coordinated by the Barcelona Supercomputing Center (BSC) and has a budget of over 14 million Euros, including over 8 million Euros funded by the European Commission, has 3 objectives:

- to develop a fully functional energy-efficient HPC prototype using low-power commercially available embedded technology
- to design a next-generation HPC system together with a range of embedded technologies in order to over-

come the limitations identified in the prototype system, and

- to develop a portfolio of Exascale applications to be run on this new generation of HPC systems.

Increase in energy-efficiency

With energy efficiency being a key issue, supercomputers are expected to achieve 200 Petaflop/s in 2017 with a power budget of 10 MW, and 1000 Petaflop/s (1 Exaflops/s) in 2020 with a power budget of 20MW. That means an increase in energy-efficiency of more than 20 times compared with the most efficient supercomputers today.

“First, we must take into account that not all energy is used for computing within the cores. In current systems the processors consume the lion’s share of the energy, often 40% or more. The remaining energy is used to power up the memory, interconnection network, and storage system. Furthermore, a significant fraction is wasted in power supply overheads, and in thermal dissipation (cooling), which do not contribute to performance at all”, says **Alex Ramirez**, leader of the Mont-Blanc project.

The system architecture in Mont-Blanc will rely on energy-efficient ARM processors, also used in embedded and mobile devices. It is expected to achieve from 4 to 10 times increase in energy-efficiency compared with current technologies.

The Mont-Blanc project will build on the experience of two previous ARM-based prototypes developed under the PRACE prototyping efforts, an ARM multicore cluster built on Tegra2 dual-core

Cortex-A9 chips, and an ARM+GPU cluster built from Tegra3 quad-core chips and

mobile (MXM) GPU accelerators.

These prototypes will provide valuable feedback for the Mont-Blanc prototype, and will enable both application and system software development while the Mont-Blanc system is being developed.

The Mont-Blanc project brings together a purely European consortium which joins industrial technology providers and research supercomputing centers: Bull, as the major HPC system vendor, ARM, as the world leader in embedded high-performance processors, and Gnodal, as interconnect partner that focuses its new product on scalability and power efficiency. Besides the technology providers, Mont-Blanc unites the supercomputing centres from the four Tier-0 hosting partners in PRACE who have leading roles in system software and Exascale application development: Germany (Forschungszentrum Jülich, BADW-LRZ), France (GENCI, CNRS), Italy (CINECA), and Spain (BSC).

They also run thousands of real applications on a daily basis on their Tier-0 and Tier-1 systems, coming from a vast number of scientific domains and serving a large community of academic and industrial users. In order to assess the different hardware and software components made available during the project, an incremental approach will be used, working on both the porting and the optimisation of small kernels, and then on real end-users scientific applications.

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